AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Previously Presented) A switch comprising:

a plurality of ports for exchanging data, and a shared-memory for enabling the exchange of data between first and second ones of said ports, said shared-memory comprising:

an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width;

circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports.

2. (Original) The switch of claim 1 and further comprising a buffer associated with each port for converting words of data from an initial bit-width to said predetermined bit width.

3. (Original) The switch of claim 1 wherein said predetermined bit-width is equal to a bit-width of certain bit width and associated overhead.

4. (Original) The switch of claim 2 wherein said initial bit-width is 48 bits and said predetermined bit-width is 384 bits.

5. (Original) The switch of claim 1 wherein said circuitry for reading and writing comprises an available address table for storing write addresses available for selection and use in writing to selected rows said array.

6. (Original) The switch of claim 5 wherein said circuitry for reading and writing further

comprises a used address table for storing addresses already used for writing data to selected rows in said array.

7. (Original) The switch of claim 1 wherein said array comprises an array of random access memory cells of the read/write classification.

8. (Currently Amended) A ~~shared-memory~~ switch, comprising:

a plurality of ports ~~for exchanging~~configured to exchange data ~~between~~ with external devices ~~associated with each of said ports~~;

~~a buffer associated with each of said ports for assembling a stream of data words being input into said switch into a single word of a predetermined width and for converting single data words of said predetermined width being output from said switch into a stream of data words;~~

a [[shared-memory]] memory ~~for effectuating a transfer of data from a first one of said ports to a second one of said ports through corresponding ones of said buffers, said shared-memory comprising~~ including a plurality of banks, each bank having an array of memory cells arranged as a plurality of rows, wherein each row comprises y number of memory cells ~~and a single column of~~ , and wherein the memory further comprises ~~and~~ circuitry ~~for selecting~~configured to select one of the plurality of rows ~~a said row~~ in response to a received address;

a buffer associated with one of the plurality of ports and configured to assemble a stream of data words, as received by the one of the plurlaity of ports, into a single word having a predetermined width, wherein the predetermined width includes x number of bits, and wherein y divided by x results in an integer greater than one;

a plurality of available address tables, each available address table ~~for maintaining~~including a queue of addresses available for writing ~~said single words of~~ data to a corresponding one of ~~said~~ the banks; and

a plurality of used address tables, each used address table ~~for maintaining~~including a queue of addresses for reading from a corresponding one of ~~said~~ the banks.

9. (Currently Amended) The switch of claim 8, wherein ~~said~~ the streams of data words comprises eight forty-eight bit words of ATM data ~~and said single words have a said predetermined width of 384 bits~~.

10. (Currently Amended) The switch of claim 8, wherein each of ~~said~~ the plurality of available address tables comprises a first-in-first-out memory.

11. (Currently Amended) The switch of claim 8, wherein each of ~~said~~ the plurality of used address tables comprises a random access memory~~,~~ ~~that performs~~configured to perform read and write operations.

12. (Currently Amended) The switch of claim 8, wherein each of ~~said~~ the banks ~~is~~ are randomly accessible.

13. (Currently Amended) The switch of claim 8, wherein each of ~~said~~ the banks are designated to store ~~stores~~ data from corresponding ~~to a selected~~ ones ~~said~~ of the ports ~~from which data is to be read~~.

14. (Currently Amended) The switch of claim 8, wherein each of ~~said~~ the banks ~~stores~~ are designated to store data from ~~corresponding to~~ more than one of the~~a~~ plurality of ports ~~from which data is to be read in a selected order~~.

15. (Currently Amended) The switch of claim 8, wherein ~~said~~ the [[shared-]]memory comprises i number of banks and ~~said~~ the switch comprises j number of ports, where i<j.

16. (Previously Presented) A digital information system comprising:

first and second resources operable to exchange data in a selected digital format; and

a digital switch comprising:

first and second ports for selectively coupling said first and second resources; and

a shared memory for enabling the exchange of data between said first and second ports as words of a predetermined word-width, said shared-memory comprising:

an array of memory cells arranged as a plurality of rows and a single column having a width equal to said predetermined word-width; and

circuitry for writing a selected data word presented at said first one of said ports to a selected row in said array during a first time period and for reading said selected data word from said selected row during a second time period to said second one of said ports.

17. (Original) The system of claim 16 wherein data are exchanged through said ports as streams of data words of an initial word-width and said switch further comprises buffers for converting data words between said initial word-width and said predetermined word-width.

18. (Original) The system of claim 16 wherein said selected digital format comprises as Asynchronous Transfer Mode digital data format.

19. (Original) The system of claim 18 wherein said predetermined word-width equals a bit-width of a user data portion of an asynchronous transfer mode information packet.

20. (Original) The system of claim 16 wherein said first and second resources are selected from the group comprising digital telephones, digital facsimile machines, digital data networks, home networks, digital private branch exchanges, workstations and video teleconferencing equipment.

21. (Original) The system of claim 16 where the data interface is selected from the group consisting of DDR (double data rate), QDR (quad data rate), Rambus.TM., and programmable bit burst length interfaces.

22-32 (Canceled)